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multifunctional and general-purpose properties.

The memory circuit may be internally programmable as to whether it is used or not. It is accordingly not necessary, when the present memory circuit is not used, to instruct that fact through an external instruction input, allowing an instruction line for the just-mentioned external input to be available for another application, followed by further improvement of multifunctional and general-purpose properties.

Furthermore, an input/output selection switch may be provided for making selectable at least part of an input of the chip control means, an input of the address buffer, and inputs and outputs of the input/output buffer. Accordingly, at least part of the input of the chip control means, the input of the address buffer, and the inputs and outputs of the input/output buffer can be directly connected to another line in the PLD other than a general line in the same PLD which is ordinarily used, such as for example a long line, a bus, and an input/output buffer, etc., allowing the general line to be employed for other applications, further improving the multifunctional and general-purpose properties. Particularly, when the input/output buffer is made selectable, direct input/output connection to the outside is possible.

Reference is made, by way of example, to the accompanying drawings, in which:-

Fig. 1 is a block diagram illustrating the arrangement of a first embodiment of a semiconductor memory circuit according to the present invention;

Fig. 2 is a block diagram illustrating the arrangement of a second embodiment of the same;

Fig. 3 is a circuit diagram illustrating the arrangement of a memory cell for use in the second embodiment; and

Fig. 4 is a block diagram illustrating an input/output selection switch for use in a third embodiment.

In a first embodiment of the present invention, an 8 kbit semiconductor memory circuit will be taken as an illustrative example to which the present invention is applied.

The circuit includes, as illustrated in Fig. 1, a chip control circuit 10 for deciding whether the circuit is to be used or not, and selecting memory function (RAM mode or FIFO mode), and the number of bits of one word on the basis of external control signals $\overline{CS}$, FOM, m0 and m1, and further receiving an external write designation (request) signal $\overline{WREQ}$ and a read designation (request) signal $\overline{RREQ}$, etc., an address buffer 12 having a function to select an effective address length among address inputs A0 - A12 set in conformity with the longest bit arrangement, on the basis of a bit construction assigned by the chip control circuit 10, an address counter 14 for counting up a write address or a read address at each write or read operation when the first-in first-out (FIFO) mode has been selected by the chip control circuit 10, memory cell arrays 16A, 16B composed of two blocks, each of which blocks includes 128 x 32 memory cells, column decoders 18A, 18B having functions of a sense amplifier and a write/read circuit, for controlling the memory cell arrays 16A, 16B on the basis of the bit construction assigned by the chip control circuit 10, a line decoder 20 having same functions as the column decoders 13A, 13B, and an input/output (I/O) buffer 22 for selecting an effective data length based on the bit construction assigned by the chip control circuit 10.

The chip control circuit 10 includes an input terminal for receiving a chip select signal CS for selecting whether the present whole chip is to be used or not, an input terminal for receiving a mode control signal FOM which is to select whether the whole chip is operated with the ordinary (S)RAM mode or with the FIFO mode, input terminals for respectively receiving an external write request signal $\overline{WREQ}$ and a read request signal $\overline{RREQ}$ when the FIFO mode has been selected, and for respectively receiving a write enable signal $\overline{WE}$ for opening an input buffer and an output enable signal $\overline{OE}$ for opening an output buffer when the RAM mode has been selected, input terminals for respectively receiving bit length select signals m0, m1 for selecting the number of bits of one word, and an output terminal for issuing an alarm signal AWNG as it is found that a read address among addresses of the address counter 14 is coincident with an address +1 which has been written recently when the FIFO mode has been selected, i.e., when an address, which has not yet been written with any information, is assigned. Here, each overlined "-" signal means that the signal is true when it is at a "0" level (low level).

The mode control signal FOM can be set to select the ordinary RAM mode when it is "0" for example while selecting the FIFO mode when "1".

The bit length select signals m0, m1 can be set to select 1 word 1 bit when they are "0, 0", 1 word 4 bits when "1, 0", 1 word 8 bits when "0, 1", and 1 word 16 bits when "1, 1", as listed in Table 1.

the use of an instruction line for the external input to other applications because there is no need of successively instructing externally that the circuit is not to be used, thereby further improving multifunctional and general-purpose properties of the circuit.

In the timing control circuit 30, the bit length select signals m0, m1 for selecting the number of bits of one word can also be set in programming memories 30B, 30C upon the programming of the whole PLD.

The memory cell array 16 is here integrally constructed differing from the case in the first embodiment. Each memory cell constituting the memory cell array 16 comprises a static RAM, which includes as illustrated in Fig. 3 for example, two information holding inverters 40, 42 and three selection transistors 44, 46, 48 for connection and separation between the memory cell and bit lines "bit" in conformity with a voltage level of word lines "word". To realize the write and read operations independently, the word lines "word" and the bit lines "bit" are independently provided for writing (word - w, bit - w, $\overline{\text{bit}}$ - w) and read out (word - r, bit - r).

In the present embodiment, when the mode control signal FOM is "0" for example, the ordinary RAM mode is selected and the address switching circuits 32A, 32B make valid the address inputs A0 - A12 from the address buffer 12. In contrast, when the mode control signal FOM is "1" for example, the FIFO mode is selected and the address switching circuits 32A, 32B make valid the address inputs from the write and read address counters 14A, 14B.

Additionally, if the write and read addresses are coincident with each other, then writing has priority.

Further, if the write address is filled up in writing, then the writing is interrupted, and if the write reset signal WRES is entered, then the writing is restarted from the oldest address for example.

For other details, the description in the first embodiment is applicable and will be omitted here.

In the present embodiment, the writing and the read out are independently executable in the FIFO mode, and hence successive operations are made possible, further improving multifunctional and general-purpose properties.

Next, a third embodiment of the present invention will be described with reference to Fig. 4.

The present embodiment additionally includes, in the same semiconductor memory circuit as the second embodiment, an input (output) selection switch 50 disposed on the input side of the address buffer 12, on the input side of the timing control circuit 30, on the input side of the input buffer 22A, and on the output side of the output buffer 22B, as illustrated in Fig. 4 as the input side of the address buffer 12 for example.

Referring to Fig. 4, the input selection switch 50 disposed on the input side of the address buffer 12 for selecting the address lines is illustrated. The switch 50 assures the connection, to the address buffer 12, of any one of, besides the general lines A0S - A12S located in the typical PLD, long lines A0V - A12V, buses A0B - A12B. and input/output blocks (IOB) A0I - A12I. Selection of such connection lines is effected upon programming for the whole PLD by setting memory values Q0, Q1 in programming memories 50A, 50B upon the programming of the whole PLD. For example, if the memory values Q0, Q1 in the programming memories 50A, 50B are "0, 0", then the general lines A0S - A12S are selected, if "0, 1", then the long lines A0V - A12V are selected, if "1, 0", then the buses A0B - A12B selected, and if "1, 1", then I0B A0I - A12I are selected.

Although the same input (output) selection switches are additionally provided on the input side of the timing control circuit 30, on the input side of the input buffer 22A, and on the output side of the output buffer 22B, the detailed description will be omitted here.

In the present embodiment, the input (excepting bit length select signals m0, m1) lines of the timing control circuit 30, the input lines of the address buffer 12, the input lines of the input buffer 22A, and the output lines of the output buffer 22B are made selectable, so that any association input/output signal can directly be inputted and outputted into and from the long line, bus, and I0B, etc., other than the general line in the typical PLD, and use of the general line to other applications is assured, further improving the multifunctional and general-purpose properties of the present memory circuit. In particular, when the I0B is made selectable, direct inputs and outputs from and to the outside is assured.

It should now be understood that although in the present embodiment all of the input of the address buffer 12, input of the timing control circuit 30, input of the input buffer 22A, and output of the output buffer 22B were made selectable, any part of those input and output may be fixed and the input (output) selection switch may be omitted.

Furthermore, although in the present embodiment, the input (output) selection switch was combined with the circuit of the second embodiment, the input (output) selection switch may be combined with the circuit of the first embodiment.

Although certain preferred embodiments have been shown and described, it should be understood that many changes and modifications may be made therein without departing from the scope of the appended claims.

filled up upon the write operation, and the write operation is restarted from the oldest address when a write reset signal is entered.

Patentansprüche

1. Halbleiter-Speicherschaltung, die die Anzahl der zu ihr gehörenden Bits und Worte ändern kann, wobei die Schaltung umfaßt

   eine Chipsteuervorrichtung (10, 30), geeignet mindestens zum Wählen der Bitanzahl eines Worts und zum Umschalten zwischen einem wahlfreien Speicherzugriffsmodus (RAM-Modus) und einem First-In-First-Out-Speichermodus;

   einen Adreßpuffer (12), der eine Funktion zum Ändern einer tatsächlichen Adreßlänge ausgehend von einem gewählten Bitmuster aufweist;

   eine mit einem Ausgang des Adreßpuffers (12) verbundene Adreßzähleinrichtung (14; 14A, 14B), geeignet zum Hochzählen einer Schreib- oder Leseadresse bei jedem Schreib- bzw. Lesevorgang, wenn die First-In-First-Out-Speicherfunktion gewählt wurde;

   ein Speicherzellenfeld (16A, 16B), das Speicherzellen enthält, die wahlweise sowohl im wahlfreien Speicherzugriffsmodus (RAM-Modus) als auch im First-In-First-Out-Speichermodus betreibbar sind;

   eine zwischen der Adreßzähleinrichtung und dem Speicherzellenfeld angebrachte Zeilen- und Spaltendecodiervorrichtung (18A, 18B, 20; 34A, 34B, 36A, 36B, 20A, 20B), geeignet zum Steuern des Speicherzellenfelds ausgehend von einem gewählten Bitmuster; und

   mit der Spaltendecodiereinrichtung (18A, 18B; 34A, 34B, 36A, 36B) der Zeilen- und Spaltendecodiervorrichtung verbundene Eingabe- und Ausgabepuffervorrichtungen (22; 22A, 22B), die eine Funktion zum Wechseln einer tatsächlichen Datenlänge aufweisen, ausgehend vom gewählten Bitmuster.

2. Schaltung nach Anspruch 1, wobei die Schreib- und Lesevorgänge unabhängig ausführbar sind, wenn der First-In-First-Out-Speichermodus gewählt wurde.

3. Schaltung nach Anspruch 1 oder 2, ferner umfassend Programmiervorrichtungen (30A), die programmierbar sind, um festzulegen, ob die Speicherschaltung selbst benutzt wird oder nicht.

4. Schaltung nach Anspruch 1, 2 oder 3, die zudem einen Eingangs-(Ausgangs-)Wahlschalter (50) umfaßt, geeignet zum Freigeben mindestens eines Teils eines Eingangs des Adreßpuffers (12) und zum Wählen von Eingängen und Ausgängen der Ein-Ausgabepuffervorrichtung (22).

5. Schaltung nach irgendeinem vorhergehenden Anspruch, wobei die Chipsteuerschaltung (10) die von der Adreßzählvorrichtung (14) gezählten Werte überwacht und ein Alarmsignal (AWNG) abgibt, wenn eine Adresse zum Lesen bezeichnet wird, auf die noch keine Information geschrieben wurde.

6. Schaltung nach Anspruch 1, weiterhin umfassend

   Schreib- und Leseadreßzähler (14A, 14B), die die Adreßzählvorrichtung bilden und getrennt bereitgestellt sind, geeignet zum unabhängigen Hochzählen der Schreib- und Leseadressen bei jedem Schreib- und Lesevorgang, wenn der First-In-First-Out-Speichermodus gewählt wurde;

   eine Schreibadressenumschaltvorrichtung (32A), geeignet zum Gültigmachen einer Adreßeingabe vom Adreßpuffer (12), wenn der Speichermodus mit wahlfreiem Zugriff (RAM-Modus) gewählt wurde, wogegen eine Adreßeingabe vom Schreibadreßzähler gültig gemacht wird, wenn der First-In-First-Out-Speichermodus gewählt wurde; und

   eine Leseadressenumschaltvorrichtung (32B), geeignet zum Gültigmachen einer Adreßeingabe vom Adreßpuffer, wenn der Speichermodus mit wahlfreiem Zugriff (RAM-Modus) gewählt wurde, wogegen eine Adreßeingabe vom Leseadreßzähler gültig gemacht wird, wenn der First-In-First-Out-Speichermodus gewählt wurde;

   Eingangs- und Ausgangspuffer (22A, 22B), die die Eingangs-Ausgangs-Puffervorrichtung bilden, die getrennt bereitgestellt sind und eine Funktion zum Wechseln einer tatsächlichen Datenlänge ausgehend von einem gewählten Bitmuster aufweisen, wobei die Eingangs-Ausgangs-Puffervorrichtung Spalten- und Zeilenschreibdecodierer (34A, 36A, 20A) und Spalten- und Zeilenlesedecodierer (34B, 36B, 20B) aufweist.

7. Schaltung nach Anspruch 6, wobei jede Speicherzelle des Speicherzellenfelds ein statischer Speicher mit wahlfreiem Zugriff (RAM) ist, aufgebaut aus Invertern (40, 42) geeignet zum Halten von Information,

mier sorti a été sélectionné; et

des moyens de commutation d'adresse de lecture (32B) pour rendre valide une entrée d'adresse dudit tampon d'adresse lorsque le mode de mémoire à accès direct a été sélectionné et rendre valide une entrée d'adresse dudit compteur d'adresse lorsque le mode de mémoire premier entré-premier sorti a été sélectionné;

des tampons d'entrée et de sortie (22A, 22B) constituant lesdits moyens de tampon d'entrée/sortie et prévus séparément, ayant une fonction qui consiste à modifier une longueur de donnée effective sur la base de la configuration de bits sélectionnée;

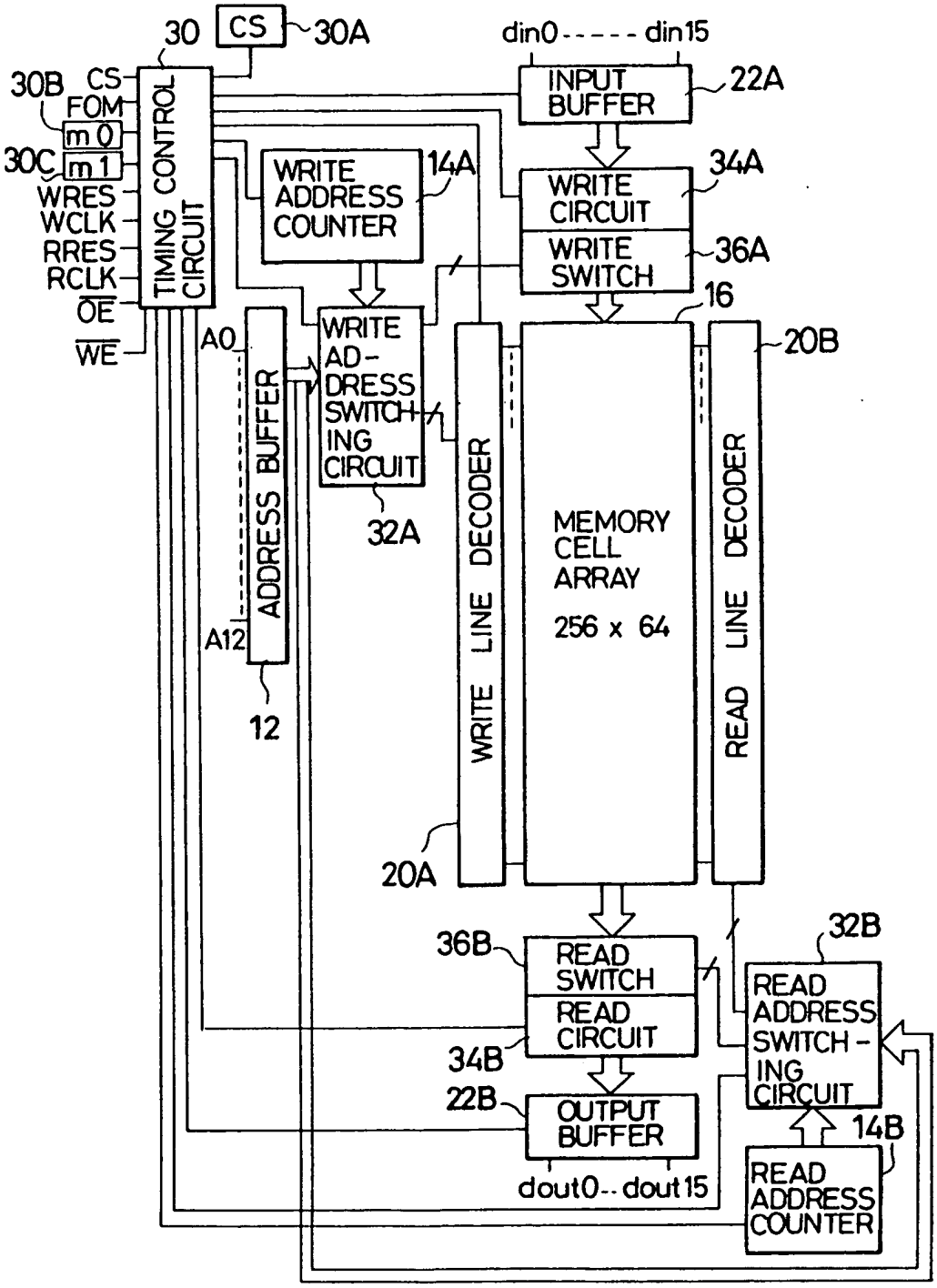
et dans lequel lesdits moyens de tampon d'entrée/sortie comprennent des décodeurs d'écriture de colonnes et de lignes (34A, 36A, 20A) et des décodeurs de lecture de colonnes et de lignes (36B, 34B, 20B).

7. Un circuit selon la revendication 6, dans lequel chaque cellules mémoire de ladite matrice de cellules mémoire est une mémoire à accès direct statique formée d'inverseurs (40, 42) pour maintenir l'information, et des transistors de sélection (44, 46, 48) pour connecter et séparer chaque cellule mémoire avec et d'avec des lignes de bits (bit - w, bit - r, $\overline{\text{bit - w}}$) conformément à un niveau de lignes de mots (word - w, word - r), les lignes de mots et les lignes de bits étant prévues indépendamment pour les opérations d'écriture et de lecture.

8. Un circuit selon la revendication 6 ou 7, dans lequel lorsque l'adresse d'écriture et l'adresse de lecture coïncident, une opération d'écriture doit être exécutée en priorité.

9. Un circuit selon l'une des revendications 6, 7 ou 8, dans lequel l'opération d'écriture est interrompue lorsque l'adresse d'écriture atteint son maximum lors de l'opération d'écriture, et l'opération d'écriture est redémarrée depuis l'adresse la plus ancienne lors de l'introduction d'un signal de réinitialisation.

FIG. 2


30
CS
30A
din0 - - - - - din15
30B
CS
FOM
m 0
30C
m 1
WRES
WCLK
RRES
RCLK
OE
WE
TIMING CONTROL CIRCUIT
INPUT BUFFER
22A
WRITE ADDRESS COUNTER
14A
WRITE CIRCUIT
34A
WRITE SWITCH
36A
16
20B
A0
A12
ADDRESS BUFFER
12
WRITE AD-DRESS SWITCH-ING CIRCUIT
32A
WRITE LINE DECODER
MEMORY CELL ARRAY
256 x 64
READ LINE DECODER
20A
36B
READ SWITCH
READ CIRCUIT
34B
22B
OUTPUT BUFFER
dout0 - - dout15
32B
READ ADDRESS SWITCH-ING CIRCUIT
14B
READ ADDRESS COUNTER